MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

(An UGC Autonomous Institution)

Approved by AICTE New Delhi & Affiliated to JNTUH

Accredited by NBA (Tier 1) and NAAC with 'A' Grade

Maisammaguda, Medchal (Dist), Hyderabad - 500100, Telangana, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech. IV Year II Semester (2025-26) Time Table	ECE- A

ROOM NO: 5205 **W.E.F: 24-11-2025**

Day/Time	9:30-10:20	10:20-11:10	11:10-11:20	11:20-12:10	12:10-1250	12:50-1:50	1:50-2:50	2:50-3:50
MONDAY	Project Stage–II		B R E A K	Project Stage–II	L U N C H	Project Stage–II		
TUESDAY	Project Stage–II			Project Stage–II		Project Stage–II		
WEDNESDAY	Project Stage–II			Project Stage–II		Project Stage–II		
THURSDAY	Project Stage–II			Project Stage–II		Project Stage–II		
FRIDAY	ESD			ISE		DIP		ISE
SATURDAY	ISE	DIP		DIP		ISE	ESD	

Class Co-ordinator(s):		M. Ramanjaneyulu
SUBJECT CODE	SUBJECT	NAME OF THE FACUTY
R22A0423	Digital Image Processing	R. Sathish Kumar
R22A0426	Embedded System Design	M. Ramanjaneyulu
R22A0335	Innovation, Start-Up & Entrepreneurship	D.Santhosh Kumar

HOD **PRINCIPAL**

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech. IV Year II Semester (2025-26) Time Table	ECE- B

ROOM NO: 5102   **W.E.F:24-11-2025**

Day/ Time	9:30-10:20	10:20-11:10	11:10-11:20	11:20-12:10	12:10-1250	12:50-1:50	1:50-2:50	2:50-3:50
MONDAY	Project Stage–II		B R E A K	Project Stage–II	L U N C H	Project Stage–II		
TUESDAY	Project Stage–II			Project Stage–II		Project Stage–II		
WEDNESDAY	Project Stage–II			Project Stage–II		Project Stage–II		
THURSDAY	Project Stage–II			Project Stage–II		Project Stage–II		
FRIDAY	ISE	DIP		DIP		ISE	ESD	
SATURDAY	ESD			ISE		DIP	ISE	

Class Co-ordinator(s):	R. Sathish Kumar
SUBJECT CODE / SUBJECT	NAME OF THE FACUTY

SUBJECT CODE	SUBJECT	NAME OF THE FACUTY
R22A0423	Digital Image Processing	R. Sathish Kumar
R22A0426	Embedded System Design	M. Ramanjaneyulu
R22A0335	Innovation, Start-Up & Entrepreneurship	D.Santhosh Kumar

HOD   **PRINCIPAL**